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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,941	01/16/2004	Charles Ray Johns	AUS920030429US1	8208

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EXAMINER	
KROFCHECK, MICHAEL C	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,941	JOHNS ET AL.	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/759,941 filed on 1/16/2004.

2. Claims 1-24 have been submitted for examination.

3. Claims 1-24 have been examined.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 13-24 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 13 recites the limitation "the reference table" in each claim. There is insufficient antecedent basis for this limitation in the claims. Did the applicant intent to state, "the page table"?

7. Claims 16, 18, 19, 21, 22-24 recite the limitation "the means for pre-loading" in each claim. There is insufficient antecedent basis for this limitation in the claims.

8. The claims not specifically mentioned are rejected because of their dependencies.

Claim Rejections - 35 USC § 101

9. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

10. Claim 24 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

11. Claim 24 is not limited to tangible embodiments and is at best directed to software, per se. The computer program code needs to be tangibly embodied on a computer readable medium.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

14. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

15. Claims 1-5, 12-16 rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (AAPA), and Hammond, US Patent 5918250.

16. With respect to claim 1, AAPA teaches of an apparatus for managing a translation mechanism in a processor architecture comprising: an execution unit for generating an effective address (fig. 1-2, items 110, 210; page 5, lines 22-26, page 6, lines 2-6; where the execution unit issues effective addresses (EA));

a translator, wherein the translator at least translates an effective address into a real address, wherein if a translation is at least not available, then the real address is unavailable (fig. 1-2, items 112, 212; page 5, line 26-page 6, line 4; page 6, lines 18-23; where the TLB searches for a translation (real address) for the EA, if it does not exist, then it is unavailable);

a miss manager, wherein the miss manager is at least configured to manage unavailable real addresses from the means for translating (fig. 1-2, item 114, 214; page 6, lines 3-8);

a storage means, wherein the storage mean at least stores a plurality of general data wherein the plurality of general data is at least referenced by real addresses (fig. 1-2, item 116, 216; page 5, lines 16-17, 24-page 6, line 7; The EA references to data in

the main storage are translated into real addresses (RA), this is done because the data in the main storage is referenced by the RA and not the EA).

AAPA fails to explicitly teach of means for pre-loading translation data. However, Hammond teaches of means for pre-loading translation data (fig. 1; items 197, 195; column 4, line 58-column 5, line 15; where the preload circuit preloads the translation attribute data and if it matches, the software TLB handler only needs to load one register).

AAPA and Hammond are analogous arts as they are both in the same field of endeavor, address translation. It would have been obvious to one of ordinary skill in the art having the teachings of AAPA and Hammond at the time of the invention to include the preload circuit, software TLB handler, and the means to use them as taught in Hammond in AAPA. Their motivation would have been to decrease the time for a TLB fill and make the process as streamlined as possible (Hammond, column 2, lines 28-31).

17. With respect to claim 12, AAPA teaches of a method for managing a translation mechanism in a processor architecture comprising: generating an effective address (fig. 1-2, page 5, lines 22-26, page 6, lines 2-6; where the execution unit issues effective addresses (EA));

translating an effective address into a real address, wherein if a translation is at least not available, then the real address is unavailable (fig. 1-2; page 5, line 26-page 6, line 4; page 6, lines 18-23; where the TLB searches for a translation (real address) for the EA, if it does not exist, then it is unavailable);

managing unavailable real addresses from the step of translating (fig. 1-2; page 6, lines 3-8);

accessing a plurality of stored general data wherein the plurality of stored general data is at least referenced by real addresses (fig. 1-2, item 116, 216; page 5, lines 16-17, 24-page 6, line 7; The EA references to data in the main storage are translated into real addresses (RA), this is done because the data in the main storage is referenced by the RA and not the EA. It is abundantly clear to one of ordinary skill in the art that this is done to access the data in the main storage).

AAPA fails to explicitly teach of pre-loading unavailable data. However, Hammond teaches of pre-loading unavailable data (fig. 1; items 197, 195; column 4, line 58-column 5, line 15; where the preload circuit preloads the translation attribute data and if it matches, the software TLB handler only needs to load one register. This is done in the occurrence of a TLB miss to load the missed data (i.e. unavailable data) into the TLB).

18. With respect to claim 2, AAPA teaches of wherein the storage means further comprises a page table (fig. 1-2, item 118, 218), wherein the page table is configured to at least provide a plurality of references to the plurality of general data (fig. 1-2; page 6, lines 3-7; the miss handler searches the page table for the translation to translate the EA, thus the page table references the data in the storage through the EAs and RAs addressing that data).

19. With respect to claim 13, AAPA teaches of the step of accessing further comprises accessing a page table, wherein the page table is configured to at least

provide a plurality of references to the plurality of general data (fig. 1-2; page 6, lines 3-7; the miss handler searches the page table for the translation (RA) to translate the EA. The RA references the data and thus the page table references the data in the storage through the EAs and RAs addressing that data).

20. With respect to claims 3 and 14, Hammond teaches of wherein the means for pre-loading further comprises a communication channel between the page table and the translator (fig. 1; column 1, lines 24-26; where the memory management unit (translator) translates the virtual address into its physical address using the page tables. Since the MMU must communicate with the page table to do such, there must be a channel of communication between them).

21. With respect to claims 4 and 15, AAPA teaches of wherein the translation mechanism further comprises a software manager coupled to the translator (fig. 1, item 102; page 5, lines 9-12; page 6, lines 9-11).

22. With respect to claims 5 and 16, AAPA teaches of the step of at least utilizing the software manager further comprises: transporting data through a data port (page 8, lines 5-6);

supplying index data from an index table to the translator (page 8, lines 8-12);

AAPA fails to explicitly teach of providing management of the means for pre-loading. However, Hammond teaches of providing management of the means for pre-loading (column 3, lines 25-36; where the processor preloads common attributes into the TLB installation registers and the operating system that controls the processor selects the attributes by storing them in a default translation register).

23. Claims 6-11 and 17-22 rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of AAPA and Hammond as applied to claim 4 and 15 respectively, and further in view of DeLano et al., US Patent 5493660.

24. With respect to claims 6-11, DeLano teaches of the translation mechanism further comprises a hardware manager coupled to the translator (fig. 1; column 5, lines 43-57; where the processor, PDIR, MMU, cache memory and hardware TLB miss handler work together as a hardware manager connected to the TLB (translator)),

the hardware manager comprises: a data port for transporting data there between (fig. 1; column 6, line 67-column 7, line 4; As the hardware TLB miss handler is directly connected to the TLB, it contains a port for accessing that connection);

an index table for supplying index data to the means for translating (fig. 3; column 5, lines 51-57; column 7, lines 8-13; where the hardware TLB miss handler searches the cache and the hardware visible portion of the PDIR (index tables) and upon finding the address, entering the information in the TLB);

Hammond teaches of means for providing management of the means for pre-loading (column 3, lines 25-36; where the processor preloads common attributes into the TLB installation registers and the operating system that controls the processor selects the attributes by storing them in a default translation register).

The combination of AAPA and Hammond, and DeLano are analogous arts as they are both in the same field of endeavor, address translation. It would have been obvious to one of ordinary skill in the art having the teachings of AAPA, Hammond, and DeLano at the time of the invention to incorporate the hardware TLB miss handler,

storing the recent translation in the cache, and the PDIR hardware viewable table as taught in DeLano into the combination of AAPA and Hammond providing for a system that uses both hardware and software TLB miss handlers. Their motivation would have been to reduce the TLB miss penalty, DeLano, abstract.

25. With respect to claims 17, 19-22, DeLano teaches of at least using a hardware manager coupled to the translator (fig. 1; column 5, lines 43-57; where the processor, PDIR, MMU, cache memory and hardware TLB miss handler work together as a hardware manager connected to the TLB (translator)),

where the used hardware manager comprises: transporting data through a data port for transporting data there between (fig. 1, 3; column 6, line 67-column 7, line 4; column 7, lines 15-17; As the hardware TLB miss handler is directly connected to the TLB, it contains a port for accessing that connection, which is used to insert entry information into the TLB);

supplying index data from an index table to the translator (fig. 3; column 5, lines 51-57; column 7, lines 8-13; where the hardware TLB miss handler searches the cache and the hardware visible portion of the PDIR (index tables) and upon finding the address, entering the information (index data) in the TLB (translator));

Hammond teaches of providing management of the means for pre-loading (column 3, lines 25-36; where the processor preloads common attributes into the TLB installation registers and the operating system that controls the processor selects the attributes by storing them in a default translation register).

26. With respect to claim 18, the combination of AAPA and Hammond teach of the limitations within as cited with respect to claim 16.

27. Claims 23-24 rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Hammond, and Belair, US Patent 6212613.

28. With respect to claims 23 and 24, AAPA teaches of a computer program product for managing a translation mechanism in a processor architecture having a computer program, the computer program comprising: computer program code for transporting data through a data port (fig. 1; page 8, lines 1-8; As the software manager contains and uses the TLB data port, it is abundantly clear to one of ordinary skill in the art that it contains code that allows it to do such);

computer program code for supplying index data from an index table to the translator (fig. 1; page 8, lines 8-14; As the software manager contains and supplies the TLB index data to the TLB (translator), it is abundantly clear to one of ordinary skill in the art that it contains code that allows it to do such);

AAPA fails to explicitly teach of, the computer program product having a medium with a computer program embodied thereon, and a computer program code for providing management of the means for pre-loading.

However, Hammond teaches of computer program code for providing management of the means for pre-loading (column 3, lines 25-36; where the processor preloads common attributes into the TLB installation registers and the operating system that controls the processor selects the attributes by storing them in a default translation register).

Belair teaches of, the computer program product having a medium with a computer program embodied thereon (fig. 1, item 28; column 5, lines 12-15; column 6, lines 36-43).

The combination of AAPA and Hammond, and Belair are analogous arts as they are both in the same field of endeavor, address translation. It would have been obvious to one of ordinary skill in the art having the teachings of AAPA and Hammond, and Belair at the time of the invention to include the programs/control code of the combination of AAPA and Hammond on a computer readable medium. Their motivation would have been to provide a way to input and potentially upgrade the code, Belair column 12, lines 43-51.

Conclusion

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

31. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

32. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Krofcheck

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